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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KOSTAK, VICTOR R	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,940	PETHER, DAVID N.	
	Examiner	Art Unit	
	Victor R. Kostak	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/27/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Regarding a first matter, pixels are not necessarily digital signals, though argued as such and said to be corroborated by the dictionary definition provided by applicant. Before television became digital as it is now accepted, the term "pixel" was coined and used throughout the earlier years of analog television (see patent 4,442,544 col. 3 lines 16-20 and *"Basic Communication Theory"* section 6.4.3 page 84, attached herewith). Pixels are not exclusively digital.

In addition, and as corroborated by applicant's submitted definition, pixels are not electrical signals that are encoded, transported, etc., as asserted by the examiner in a previous Office action. Pixels are the actual elements generated by an image signal typically by a photo-optical device (e.g. camera) and data elements displayed by a receiver-end display device. The signals *representing* the pixels are that which are encoded, transmitted, modulated, etc. Applicant's submitted definition states that pixels are square or rectangular in area located at specific x and y positions in the image plane, which supports the examiner's description, and which is consistent with the description given in *"Basic Communication Theory"* cited above.

The text cited in the patent attached herewith further corroborates the examiner's clarification regarding the fact that pixels are not transferred but signals representing pixels are, and which can be analog.

In view of all this, it accordingly follows that the three inputs (i.e. video signals) to component 68 of Bilbrey are analog signals representative of pixels, which is broadly supported by the rest of his disclosure. (Banker was also discussed in the last Office action for corroboration regarding this issue.)

2. Claim 8 is now objected to because of the following informalities: "said memory" now lacks antecedent basis because "a memory" was removed from base claim 1. Appropriate correction is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-8, 10-15, 17-19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (of record).

The correlation of applicant's claims to Chen will be expanded herein to the explanation presented in the last Office action, to assist applicant in following along.

Reviewing Chen (noting particularly Figs. 1-3, 6 and 9), his system includes a first circuit comprising DRAM 308 (which contains both pixel data and processing commands: section 301) calculates and writes a signal having a first resolution and plural pixel data into the memory portion of the DRAM in response an input signal having a second resolution comprising plural pixels read from the memory with associated control signals (carried out by blitter (block-move) engine 906; and a second circuit ASIC 200 used to generate the control signals in response to the DRAM commands (i.e. the first circuit) and to (at least) one input parameter such as scaling factor (additionally noting host CPU 303 in Fig. 3), which results in the input signal to be scaled and filtered (i.e. alpha blended), and which conversion involves the input pixels as contributing

to the output pixels of the converted signal (e.g. col. 4 lines 8-22; col. 5 lines 38-50; col. 6 lines 57-61; col. 7 lines 58-65).

Applicant argues that Chen appears silent on an input signal being received a scan line at a time (new language added by amendment). Applicant further argues that no instance of scan lines in Chen has been cited (assumedly by the examiner), but such has only been claimed in this instant amendment. Applicant yet further points out that the words "scan" and "lines" are not found in Chen.

The examiner counters by stating that one of ordinary skill in the art has no need to see the word "scan" or "line" to very readily see that both "scan" and "lines" are inherent in Chen, immediately by knowing that television signals, image arrays, pixel processing, MPEG, image memory addressing and reading and writing, and other television and graphics aspects and parameters are disclosed. Applicant is informed that every single term associated with a directly related aspect of these video concepts does not need to be explicitly recited. The examiner notes that a power supply is not recited in Chen's disclosure. That does not mean that a power supply therefore cannot be involved in his system. The examiner similarly points out that applicant does not disclose a power supply, which means that his system cannot work. The examiner however did not reject his claims under 35 USC 101 and object to his disclosure under 35 USC 112 1st paragraph because no power supply has been disclosed. Some things are of course inherent.

Applicant also argues that Chen is silent regarding a first circuit configured to scale and filter the input signal, because no citation (again, presumably by the examiner) has been provided for scaling. On the contrary, the last Office action cited col. 5 lines 38-50 and col. 6 lines 57-61 (evident from the above discussion on Chen repeated from the last Office action), which cover

scaling. Furthermore, applicant's citation of Chen *preferring* software to perform scaling is not the same as Chen stating that scaling is done *exclusively* by software. "Preferably" by definition means that other means can be used, therefore being an explicit allowance by Chen to use other non-software means (namely firmware or other hardware), though less in desirability. Moreover, and as applicant notes, host CPU 303 runs the software. That circuit component therefore performs scaling according to the software it runs.

The first circuit of Chen that carries out the scaling and filtering (i.e. alpha blending) is met by the composite arrangement comprising host CPU 303 shown as connected to DRAM 308 in Fig.1.

Applicant's objection to the examiner equating CPU 303 of Chen with the microprocessor being coupled to the second circuit through a bus, is explained as follows. Claim 22 only states that a microprocessor s coupled to the second circuit through a bus. That the microprocessor is part of or separate from any previously recited or additional circuit is not recited. That CPU 303 is part of the first circuit (so explained by the examiner in the rejection) does not disallow it from being considered connected to the second circuit (i.e. the ASIC 200 shown in Fig. 3) by way of a bus 305/307.

Regarding applicant's contention that Chen does not disclose his apparatus as comprising a portion of a block move engine is countered by realizing that blitter engine 304 (as noted in the last Office action) is part of the apparatus. (Section [0003] in the publication of David Pether cited herein admits that block move engines are also known as bit blitters or blitting engines). Containing an entire block move engine covers containing a portion of it. Applicant's statement that such a block move engine that has a second circuit coupled to a microprocessor through a

bus is not completely accurate. Claim 1 only recited that the apparatus comprise a portion of a block move engine (the apparatus includes both first and second circuits), and claim 22 only states that a microprocessor is coupled to the second circuit through a bus. These limitations, as explained, are met.

Returning to the newly recited input signal being received a scan line at a time, Chen does not give extensive details of his data transfer from one component to another. Nonetheless, it would have been clearly obvious to receive the input signal one line at a time from any video source (Chen discloses MPEG video streams, digitized analog video sent to video capture 202, and the application to cable TV as an example), for the clear purpose of keeping up with any incoming serial image stream that comprises two-dimensional image frames. The standard order of data transfer, storage or presentation of image data to a processing or display device (i.e. following the two-dimensional raster scan) normally involves pixels per line, lines per frame (or field) and sequential frames that constitute an image sequence, and such presentation of a two-dimensional image sequence to the memory (or other components of Chen) would have been obvious to use which would thereby provide data in a continuous fashion and in line with the a continuous stream from which the data is supplied, such as is more specifically disclosed by McInnis (e.g. Fig. 31; col. 6 lines 45-53; col. 7 lines 2-12; col. 8 lines 3-11; col. 9 lines 7-16), who also discloses a blitter engine (col. 9 lines 14-16) in his image data processor, e.g. thereby meeting claims 1 and 12.

It is noted that applicant has not addressed the rejections of the dependent claims separately (except for claim 22, apparently relying on the basis of the patentability of the

independent claims). The previous rejections thereto accordingly still apply, and are therefore repeated as follows, from the last Office action.

As for claim 13, although Chen discloses element 304 or 906 as a blitter engine (block engine), it would have been obvious to consider the associated elements (i.e. CPU 303 and ASIC) as an overall arrangement designated as a block move arrangement. (It is noted that applicant considers his block engine as including CPU 100 as part of his overall block engine arrangement.)

As for claims 2, 3, 14 and 15, the input signal can comprise color components with an alpha blend values (e.g. RGB: col. 7 lines 60-63).

Regarding claims 6 and 17, the system is arranged and intended to operate on multiple blocks (noting the operation of Fig. 9, for example.

Since Chen incorporates a blitter engine, which inherently moves blocks of data at a time, it would have been obvious to any group of data that is a factor of the whole image frame, such as a line (Fig. 6 depicts various sections for special effects; Fig. 9 depicts whole frames), thereby meeting claims 7 and 18. Such would have been obvious in further view of MacInnis for the reasons given above regarding transfer of data n a line-by-line fashion.

As for claims 8 and 19, the writing back into the memory (as shown in Fig. 9) would accordingly be carried out per line to complete the entirety of the frame conversion.

As for claims 10 and 11, the system operates on the pixel data of the input signal to generate the converted output signal (in a scaled and/or alpha-blended format).

Considering claim 22, a CPU 303 is connected to the second circuit by way of a bus 305/307, as was explained above

4. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Bilbrey et al. (of record).

Chen discloses scaling (e.g. col. 5 lines 47-48; col. 6 lines 57-61) which inherently involves altering the dimensions in both the horizontal and vertical directions, but does not provide specific details.

It would have been obvious to convert the first dimension and then the second as taught by Bilbrey (e.g. col. 47 line 32+) to complete the scaling for the clear purpose of providing the second dimension with already converted data, and for dedicating specific processing per operation.

5. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Watson et al. (of record).

It would also have been obvious to manipulate the data as so preferred (suggested by Chen in general terms by including special effects), such as by filtering data (besides the blending filtering), in order to further alter the image to achieve any desirable effect, such as to enhance the image as taught by Watson (col. 6 lines 41-48), who also incorporates a blitter engine 322.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is 703 305-4374. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on 703 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 308-HELP.

Victor R. Kostak
Primary Examiner
Art Unit 2614

VRK